### FACULTY OF COMPUTING AND INFORMATION TECHNOLOGY

### CSC 1104: COMPUTER ORGANIZATION AND ARCHITECTURE

**Coursework**

1. (a) How does a half adder differ from a Full Adder?

(b) (i) What is a multiplexer? (ii) Draw a 1-3 demultiplexer.

(iii) How many control lines would you need to construct 30-1 Multiplexer?

2. Assume the inputs for the J-K flip flop are changing with time as shown on the diagram below, draw corresponding timing diagrams for the Q outputs assuming that it is:

(i) An ordinary flip-flop (a latch)

(ii) A positively edge triggered flip-flop

(iii) A negatively edge triggered flip-flop.

C

J

K

1. Assume the following inputs for the D flip-flop

**D** 0 1 0 1 1 0 1 0 0

**C** 0 1 1 1 0 0 1 1 0

1. Draw the corresponding timing diagrams for these inputs.
2. Assume that the output Q is initially in a state of 0, draw a corresponding timing diagram for the Q output.
3. Assume that it is a negatively edge triggered flip-flop and draw the corresponding timing diagram for the Q output.
4. (a) (i) What are Shift Registers?

(ii) Give any two uses of Shift Registers

(b) Assume the contents of the accumulator register are 0 1 1 1 0 0 0 1 and a carry flag of 0, state the new contents of the register and the value of the carry flag when the following operations are performed:

(i) RLC (ii) RRC (iii) RAL (iv) RAR

(c) Multiply the binary numbers 1101 and 101 by using a bit shifting method.

(d) Assume the following inputs for the T flip flop and list the corresponding Q outputs assuming that the initial state of Q was 1.

**T** 0 0 1 1 1 0 1 0 0 1

(5) (a) Draw a well labeled diagram of a three bit register.

(b) Define the following terms in Data Transmission

(i) Handshaking (ii) Synchronous Data Transfer

(c) An 8 bit register is loaded as shown below. Determine its contents when given a

0 1 1 0 1 1 1 0

(i) Left shift (ii) A left rotation